

REMARKS

In the above-identified Office Action the Title of the invention was objected to as not being descriptive. Accordingly, by this response the Title has been amended and is now believed to be in good form. Also, the Abstract was objected to but has now been amended in a manner which is believed to overcome the objections.

Furthermore, the claims were all rejected as being anticipated by the cited Tashiro reference. However, by this response the terms of the claims have been clarified so that such claims are believed to be allowable over the cited Tashiro published patent application, and over the prior art to be cited in this application in an Information Disclosure Statement, for the reasons set forth below.

In particular, the features of the present invention which are required in amended independent Claim 1 are not disclosed by the cited Tashiro reference. Specifically, at page 3 of the Office Action, the Examiner refers to pertinent portions of that reference as follows:

“a plurality of capacitor (i.e. capacitor C_{PD} and capacitor C_{FD}) which receive signals from said plurality of pixels at first terminals (i.e. ϕRES and ϕSEL from vertical scanning circuit) (see [0074] and figure 10)

a plurality of clamping switches (i.e. a transfer switch M1, a reset switch M2, and a selection switch M3) for setting a second terminal of each of said plurality of capacitor (i.e. C_{PD} and C_{FD}) into a predetermined electric potential ([0074])

a plurality of first storing units (i.e. switch M8 plus holding capacitor CH1) for storing signals from said second terminals of said plurality of capacitor ([0075] and figure 10)

a plurality of second storing units (i.e. switch M11 plus holding capacitor CH2) for storing signals from said second terminals of said plurality of capacitor ([0075] and figure 10)”

From these statements it appears that the Examiner reads the claimed “plurality of capacitors” on capacitors C_{PD} and C_{FD} of the reference. However, assuming that the plurality of capacitors of the present invention correspond to the capacitor C_{PD} and capacitor C_{FD} , the claimed “first terminals” should be read on respective terminals of these capacitors C_{PD} and C_{FD} , which are connected to the gate terminal of a MOS transistor M4. This readily implies that the claimed “second terminals” should also be read on respective terminals of the capacitor C_{PD} and capacitor C_{FD} , which are grounded. Thus, it is incorrect to read the claimed clamping switches on MOS transistors M1, M2, and M3 of the reference of Tashiro as in the Office Action, since independent Claim 1 clearly states that a plurality of clamping switches set the second terminal of each of the plurality of capacitors to a predetermined electric potential, and the switches M1, M2, and M3 of Tashiro are rather arranged to connect to the “first terminals” of the capacitor C_{PD} and capacitor C_{FD} . In addition, the Office Action reads the claimed first and second storing units on “switch M8 plus holding capacitor CH1” and “switch M11 and holding capacitor CH2” of the reference, respectively. This is also incorrect because independent Claim 1 clearly requires

that the first and second storing units store signals from the “second terminal” of the capacitor, whereas the holding capacitors CH1 and CH2 are arranged to store signals from the “first terminal” of the capacitor C_{PD} and capacitor C_{FD} .

In view of the foregoing, the Office Action’s comparison of Claim 1 to the cited Tashiro reference is not reasonable, and the present invention as set forth in amended independent Claim 1 is patentably distinct over Tashiro.

For these reasons it is believed that the claims as now presented are allowable, and the issuance of a Notice of Allowance is solicited.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,

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